Claims

What is claimed is:

[c1]   A method for synchronizing a data signal and a clock signal, comprising:

generating a first intermediate data signal that lags the data signal;

generating a second intermediate data signal that lags the first intermediate data signal; and

generating an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal.

[c2]   The method of claim 1, wherein generating the output signal is controlled by a synchronization signal.

[c3]   The method of claim 2, wherein the synchronization signal controls the output signal with a multiplexor.

[c4]   The method of claim 1, wherein the first intermediate data signal is generated by a flip-flop.

[c5]   The method of claim 1, wherein the first intermediate data signal lags the data signal.

[c6]   The method of claim 1, wherein the second intermediate data signal is generated by a latch.

[c7]   The method of claim 1, wherein the second intermediate data signal lags the first intermediate data signal by one half of a clock cycle.

[c8]   The method of claim 2, wherein the synchronization signal is activated after the second intermediate data signal is generated.

[c9]   A method for synchronizing a data signal and a clock signal, comprising:

step of generating a first intermediate data signal that lags the data signal;

step of generating a second intermediate data signal that lags the first intermediate data signal; and

step of synchronizing the data signal with the clock signal by combining the duration of the first intermediate data signal and the duration of the second intermediate data signal.

[c10]   An apparatus for synchronizing a data signal and a clock signal, comprising:

a first data storage device that generates a first intermediate data signal that lags the data signal;

a second data storage device that generates a second intermediate data signal that lags the first intermediate data signal; and

a multiplexor that generates an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal.

[c11]   The apparatus of claim 10, wherein the first data storage device is a flip-flop.

[c12]   The apparatus of claim 10, wherein the first intermediate data signal lags the data signal.

[c13]   The apparatus of claim 10, wherein the second intermediate data signal lags the first intermediate data signal by one half of a clock cycle.

[c14]   The apparatus of claim 10, wherein the multiplexor is controlled by a synchronization signal.

[c15]   The apparatus of claim 14, further comprising:

a synchronization control signal generator that delays generation of the

synchronization signal until after generation of the second intermediate data signal.

[c16] The apparatus of claim 10, further comprising:

a scanning input device that scans a test pattern to the second data storage device during a testing operation.

[c17] The apparatus of claim 16, wherein the scanning input device is a multiplexor.

[c18] The apparatus of claim 17, wherein the multiplexor is controlled by a scanning enablement signal.

[c19] An apparatus for synchronizing a data signal and a clock signal, comprising:

means for generating a first intermediate data signal that lags the data signal;

means for generating a second intermediate data signal that lags the first intermediate data signal; and

means for generating an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal.

[c20] The apparatus of claim 19, further comprising:

means for scanning in a test data sequence.